WHAT IS CLAIMED IS:

1. A control circuit for a memory device, comprising:

an inverter which inverts all bits of data read out from the memory device; and

a decoder which executes error correction and decoding for an output of the inverter.

2. The control circuit according to claim 1, wherein the decoder detects that there is no error for an inverted value of all bits of an initial value after data in the memory device is erased.

3. The control circuit according to claim 1, wherein the memory device comprises a nonvolatile semiconductor memory device.

4. A control circuit for a memory device, comprising:

a first inverter which inverts all bits of data to be written into the memory device;

an encoder which executes error correction and coding for an output of the first inverter;

a second inverter which inverts all bits of data to be output from the encoder and writes the inverted data into the memory device;

a third inverter which inverts all bits of data read out from the memory device; and

a decoder which executes error correction and decoding for an output of the third inverter.

5. The control circuit according to claim 4, wherein a coding method of the encoder is a method in which the decoder detects that there is no error for an inverted value of all bits of an initial value after data in the memory device is erased.

6. The control circuit according to claim 4, wherein the decoder detects that there is no error for an inverted value of all bits of an initial value after data in the memory device is erased.

7. The control circuit according to claim 4, wherein the memory device comprises a nonvolatile semiconductor memory device.

8. A memory controller for a memory device, comprising:

a buffer which holds data temporarily;

a first inverter which inverts all bits of data to be written from the buffer into the memory device;

an encoder which executes error correction and coding for an output of the first inverter;

a second inverter which inverts all bits of data to be outputted from the encoder and writes the inverted data into the memory device;

a third inverter which inverts all bits of data read out from the memory device; and

a decoder which executes error correction and decoding for an output of the third inverter.

9. The memory controller according to claim 8,

wherein a coding method of the encoder is a method in which the decoder detects that there is no error for an inverted value of all bits of an initial value after data in the memory device is erased.

10. The memory controller according to claim 8, wherein the decoder detects that there is no error for an inverted value of all bits of an initial value after data in the memory device is erased.

11. The memory controller according to claim 8, further comprising a selector which selectively supplies an output of the buffer and an output of the encoder to the memory device.

12. The memory controller according to claim 8, wherein the memory device comprises a nonvolatile semiconductor memory device.